CLAIMS

[Claim(s)]
[Claim 1] The first processing circuit and the second processing circuit to which common supply voltage is supplied are provided, and it is the integrated circuit device which operation mode and a standby mode can switch freely as a mode of operation. As for said second processing circuit, supply voltage is supplied by both operation mode and the standby mode. Said first processing circuit is supplied in operation mode, and supply of supply voltage is suspended by the standby mode. Said second processing circuit controls electrical-potential-difference supply in said first processing circuit corresponding to this mode of operation. The integrated circuit device characterized by the thickness of the gate dielectric film of the second transistor which said second processing circuit possesses being thicker than the thickness of the gate dielectric film of the first transistor which said first processing circuit possesses.
[Claim 2] The first processing circuit and the second processing circuit to which common supply voltage is supplied are provided, and it is the integrated circuit device which operation mode and a standby mode can switch freely as a mode of operation. The first processing circuit possessing the first transistor which gate dielectric film is formed by the predetermined thickness a, and drives only operation mode with the predetermined electrical potential difference A, The second processing circuit possessing the second transistor which gate dielectric film is formed by the predetermined thickness b, and is driven by both operation mode and the standby mode with the predetermined electrical potential difference B, The integrated circuit device with which are satisfied of the relation which it provides and said Thickness a and b and said electrical potential differences A and B become a<bA=B.
[Claim 3] The first processing circuit and the second processing circuit to which common supply voltage is supplied are provided, and it is the integrated circuit device which operation mode and a standby mode can switch freely as a mode of operation. The first processing circuit possessing the first transistor which gate dielectric film is formed by the predetermined thickness a, and drives only operation mode with the predetermined electrical potential difference A, The second processing circuit possessing the second transistor which gate dielectric film is formed by the predetermined thickness b, and is driven by both operation mode and the standby mode with the predetermined electrical potential difference B, The integrated circuit device with which are satisfied of the relation which the third processing circuit possessing the third transistor which gate dielectric film is formed by the predetermined thickness c, and is driven on the predetermined electrical potential difference C is provided, and said thickness a-c and said electrical-potential-difference A-C become a<b<cA=B<C.
[Claim 4] The first processing circuit possessing the first transistor which gate dielectric film is formed by the predetermined thickness a, and is driven on the predetermined electrical potential difference A, The second processing circuit possessing the second transistor which gate dielectric film is formed by the predetermined thickness b, and is driven on the predetermined electrical potential difference B, The integrated circuit device with which are satisfied of the relation which

the third processing circuit possessing the third transistor which gate dielectric film is formed by the predetermined thickness c, and is driven on the predetermined electrical potential difference C is provided, and said thickness a-c and said electrical-potential-difference A-C become a<b<cA=B<C.

[Claim 5] The integrated circuit device according to claim 2 or 3 with which said second processing circuit controls the existence of actuation of said first processing circuit.

[Claim 6] Said second processing circuit is an integrated circuit device given in claim 1 which will start electrical-potential-difference supply in said first processing circuit if the external input of a Sadanobu Tokoro number is detected to a standby mode thru/or any 1 term of 3.

[Claim 7] An integrated circuit device given in claim 1 to which the gate dielectric film of said first transistor consists of thermal oxidation film which grew up to be the front face of a semi-conductor substrate, and the gate dielectric film of said second transistor becomes the front face of said semi-conductor substrate with which at least one of an argon, fluorine, and the fluorides was poured in from the gate dielectric film of said first transistor, and the thermal oxidation film which grew up to be coincidence thru/or any 1 term of 6.

[Claim 8] An integrated circuit device given in claim 1 to which the gate dielectric film of said second transistor consists of thermal oxidation film which grew up to be the front face of a semi-conductor substrate, and the gate dielectric film of said first transistor becomes the front face of said semi-conductor substrate with which at least one side of an indium and nitrogen was poured in from the gate dielectric film of said second transistor, and the thermal oxidation film which grew up to be coincidence thru/or any 1 term of 7.

[Claim 9] An integrated circuit device given in claim 1 to which said supply voltage is supplied from the dc-battery of another object thru/or any 1 term of 8.

[Claim 10] The power source which possesses the first processing circuit and the second processing circuit to which common supply voltage is supplied, is the electronic-circuitry device which operation mode and a standby mode can switch freely as a mode of operation, and supplies supply voltage to the second processing circuit for a start [said], The dc-battery which supplies body power to this power source, and the electric power switch which turns on/switches [off] the electric power supply of this dc-battery, Provide and, as for said second processing circuit, the firm gas of the supply voltage is carried out to the ON state of said electric power switch. As for said first processing circuit, by the standby mode, supply of supply voltage is suspended also for the ON state of said electric power switch. The electronic-circuitry device characterized by the thickness of the gate dielectric film of the second transistor which said second processing circuit possesses being thicker than the thickness of the gate dielectric film of the first transistor which said first processing circuit possesses.

[Claim 11] The electronic-circuitry device possessing the low-battery power source which is the electronic-circuitry device which operation mode and a standby mode can switch freely as a mode of operation, and supplies an electrical potential difference A (=B) to the second processing circuit for a start [of an integrated circuit device according to claim 3 and this integrated circuit device], the high-voltage power source which supply an electrical potential difference C to said third processing circuit, and the notice means of data which give the data notice of the predetermined data which can judge the necessity of actuation of said first processing circuit in said second processing circuit.

[Claim 12] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and a resist mask is formed in the location of the third processing circuit for a start [of the front face of this thermal oxidation film / said]. At least one of an argon, fluorine, and the fluorides is poured into said thermal oxidation film of the location of said second processing circuit exposed from this resist mask. Said thermal oxidation film of the location of the second processing circuit is removed for a start [said] after this impregnation. The thermal oxidation film is

grown up throughout the front face of said semi-conductor substrate with which the thermal oxidation film grew up to be the location of said third processing circuit, and said impregnation was performed in the location of said second processing circuit. this thermal oxidation film -- the [said / the first transistor and / said] -- the circuit manufacture approach in which the gate electrode of the 2 third transistor was formed.
[Claim 13] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and a resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film of the location of the second processing circuit is removed for a start [said] which has been exposed from this resist mask. A resist mask is formed in the location of said second processing circuit where this thermal oxidation film was removed. At least one side of an indium and nitrogen is injected into said semi-conductor substrate of the location of said first processing circuit exposed from this resist mask. after this impregnation, said resist mask is removed and the thermal oxidation film is grown up throughout the front face of said semi-conductor substrate -- making -- this thermal oxidation film -- the [said / the first transistor and / said] -- the circuit manufacture approach in which the gate electrode of the 2 third transistor was formed.
[Claim 14] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the thermal oxidation mask which prevents thermal oxidation is formed in the location of said first processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of said semi-conductor substrate of the location of the 2 third processing circuits. the [which has been exposed from this thermal oxidation mask / said] -- A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film of the location of said second processing circuit exposed from this resist mask and said thermal oxidation mask is removed. the [which removed said resist mask and has been exposed from said thermal oxidation mask after removal of this thermal oxidation film / said] -- the thermal oxidation film is grown up to be the location of the 2 third processing circuits -- making -- said thermal oxidation film -- the [said / the first transistor and / said] -- the circuit manufacture approach in which the gate electrode of the 2 third transistor was formed.
[Claim 15] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the thermal oxidation mask which prevents thermal oxidation is formed in the location of said second processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of said semi-conductor substrate of the location of the third processing circuit for a start [said] which has been exposed from this thermal oxidation mask. A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film of the location of said first processing circuit exposed from this resist mask and said thermal oxidation mask is removed. the [which removed said resist mask and has been exposed from said thermal oxidation mask after removal of this thermal oxidation film / said] -- the thermal oxidation film is grown up to be the location of the 1 third processing circuit -- making -- said thermal oxidation film -- the [said / the first transistor and / said] -- the circuit manufacture approach in which the gate electrode of the 2 third transistor was formed.
[Claim 16] The circuit manufacture approach according to claim 14 or 15 which forms said thermal oxidation mask by the conductive layer, and formed the gate electrode of said first transistor at least by this conductive layer.
[Claim 17] The circuit manufacture approach according to claim 16 which formed the conductive layer of said thermal oxidation mask by the polish recon film.

[Claim 18] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said first processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. the [which has been exposed / said] -- A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said second processing circuit exposed from this resist mask, and said first polish recon film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. after removal of this thermal oxidation film -- said resist mask -- removing -- the [said] -- The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. A resist mask is formed in the location of the 2 third processing circuits. the [of the front face of this second polish recon film / said] -- Said second polish recon film of the location of said first processing circuit exposed from this resist mask is removed. Remove said thermal oxidation film of the location of said first processing circuit exposed by this removal, and said first polish recon film is exposed. Said resist mask is removed from the location of the 2 third processing circuits, and said second polish recon film is exposed. the [said] -- While carrying out patterning of said first polish recon film of the location of said first processing circuit and forming the gate electrode of said first transistor the [said] -- said second polish recon film of the location of the 2 third processing circuits -- patterning -- carrying out -- the [said] -- the circuit manufacture approach in which the gate electrode of the 2 third transistor was formed.

[Claim 19] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said second processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said] which has been exposed. A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said first processing circuit exposed from this resist mask, and said first polish recon film. Remove said resist mask after removal of this thermal oxidation film, and the thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said]. The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. A resist mask is formed in the location of the third processing circuit for a start [of the front face of this second polish recon film / said]. Said second polish recon film of the location of said second processing circuit exposed from this resist mask is removed. Remove said thermal oxidation film of the location of said second processing circuit exposed by this removal, and said first polish recon film is exposed. Remove said resist mask from the location of the third processing circuit for a start [said], and said second polish recon film is exposed. While carrying out patterning of said first polish recon film of the location of said second processing circuit and forming the gate electrode of said second transistor The circuit manufacture approach which carries out patterning of said second polish recon film of the location of the third processing circuit for a start [said], and formed the gate electrode of the third transistor for a start [said].

[Claim 20] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said first processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. the [which has been exposed / said] -- A resist mask is

formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said second processing circuit exposed from this resist mask, and said first polish recon film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. after removal of this thermal oxidation film -- said resist mask -- removing -- the [said] -- The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. The gate electrode of the 2 third transistor is formed. while removing this second polish recon film from the location of said first processing circuit -- the [said] -- the location of the 2 third processing circuits -- patterning -- carrying out -- the [said] -- the [said] -- the circuit manufacture approach which formed the resist mask in the location of the 2 third processing circuits, carries out patterning of said first polish recon film of the location of said first processing circuit exposed from this resist mask, and formed the gate electrode of said first transistor.

[Claim 21] It is the circuit manufacture approach of manufacturing an integrated circuit device according to claim 3 or 4. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said second processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said] which has been exposed. A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said first processing circuit exposed from this resist mask, and said first polish recon film. Remove said resist mask after removal of this thermal oxidation film, and the thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said]. The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. While removing this second polish recon film from the location of said second processing circuit, carry out patterning for a start [said] in the location of the third processing circuit, and the gate electrode of the third transistor is formed for a start [said]. The circuit manufacture approach which formed the resist mask in the location of the third processing circuit for a start [said], carries out patterning of said first polish recon film of the location of said second processing circuit exposed from this resist mask, and formed the gate electrode of said second transistor.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the circuit manufacture approach of manufacturing

the integrated circuit device possessing two or more processing circuits, the electronic-circuitry device possessing this integrated circuit device, and its integrated circuit device.

[0002]

[Description of the Prior Art] The integrated circuit device possessing current and two or more processing circuits is produced commercially as an one chip microcomputer etc., and such an integrated circuit device is used for electronic-circuitry devices, such as a portable telephone.

[0003] When it is the electronic-circuitry device which a user carries like a portable telephone, a dc-battery will be inevitably used as a power source, but since small lightweight-ization is also required, the dc-battery is also formed into small lightweight. And yet, since use of long duration is also required, reduction of power consumption is demanded of the integrated circuit device at the degree of pole. Furthermore, in order to carry out digital processing of the sound signal on real time in the case of the portable telephone of a digital method, high-speed operation is also demanded of the integrated circuit device.

[0004] In the case of a portable telephone, in order to stand by to arrival of the mail, it is necessary to always operate but, and all the parts do not always need to be operating. So, in integrated circuit devices, such as a current portable telephone, power-saving is realized by operating only a necessary minimum processing circuit at the time of standby.

[0005] Furthermore, what is necessary is just to raise the driver voltage of the transistor of the processing circuit, in order to accelerate actuation of an integrated circuit device. However, when driver voltage was raised simply, power consumption increased inevitably, and since the working speed of a transistor will fall if driver voltage is reduced, high-speed operation has also been realized, making the ON state current increase and reducing power consumption by thin-shape-izing the gate dielectric film of a transistor, while reducing driver voltage.

[0006]

[Problem(s) to be Solved by the Invention] By electronic-circuitry devices, such as the conventional portable telephone, high-speed operation is realized by reducing driver voltage, while thin-shape-izing the gate dielectric film of a transistor as mentioned above, reducing the power consumption of an integrated circuit device, and power-saving is further realized by operating only a necessary minimum processing circuit at the time of standby.

[0007] However, if the thickness of the gate dielectric film of a transistor is decreased, even if it reduces driver voltage so that a working speed may not change, a gate leakage current will increase. For example, as for the gate leakage current between a gate electrode and a semi-conductor substrate, driver voltage is set to 10 (pA) by 1.2 (V) when 20 (A) and gate length are [0.1 (micrometer) and gate width] 10 (micrometer) for the gate-dielectric-film thickness of a transistor, as shown in drawing 17 .

[0008] Since driver voltage is always especially impressed in a CMOS (Complementary Metal Oxide Semiconductor) circuit between one gate electrode of the MOS transistor of n mold and p mold, and a semi-conductor substrate, a gate leakage current will always be generated. For a certain reason, in a current integrated circuit device, the gate leakage current cannot disregard accumulating millions of transistors, either. For example, when there are 5 million CMOS transistors, the gate leakage current of the sum total is set also to 25 (muA) at the maximum.

[0009] Therefore, even if it thin-shape-izes the gate dielectric film of the transistor of an integrated circuit device while reducing supply voltage in order to realize high-speed operation, reducing the power consumption at the time of actuation as mentioned above, the gate leakage current of a transistor will increase and it becomes difficult to reduce power consumption good also in the time of standby as a result. Although what is necessary is just to increase the thickness of the gate dielectric film of the transistor of an integrated circuit device in order to reduce the gate leakage currents of a transistor, now, operating at a high speed becomes difficult.

[0010] This invention is made in view of the above technical problems, and it aims at offering at least one of the circuit manufacture approach **s which manufacture the integrated circuit device

which can operate at a high speed by the small current, the electronic-circuitry device possessing this integrated circuit device, and its integrated circuit device at the time of actuation, reducing the power consumption at the time of standby.

[0011]

[Means for Solving the Problem] The first integrated circuit device of this invention possesses the first processing circuit and the second processing circuit to which common supply voltage is supplied, and is an integrated circuit device which operation mode and a standby mode can switch freely as a mode of operation. As for said second processing circuit, supply voltage is supplied by both operation mode and the standby mode. Said first processing circuit is supplied in operation mode, and supply of supply voltage is suspended by the standby mode. The thickness of the gate dielectric film of the second transistor which said second processing circuit possesses is thicker than the thickness of the gate dielectric film of the first transistor which said second processing circuit controls electrical-potential-difference supply in said first processing circuit corresponding to this mode of operation, and said first processing circuit possesses.

[0012] Therefore, with the integrated circuit device of this invention, the first transistor and the second transistor from which the thickness of gate dielectric film is different drive with the same supply voltage. Since gate dielectric film does not have ****** as for the second transistor, although actuation is a low speed, a standby mode is also driven in the condition with a very small gate leakage current. Since the gate dielectric film of the first transistor is the maximum **, although a gate leakage current is not very small, only operation mode is driven in the condition of operating at a high speed. In addition, in order to simplify explanation here, in various kinds of thin films which make reference by each invention, thickness calls the thickest thing ** thickness and calls the thinnest thing the maximum **.

[0013] The second integrated circuit device of this invention possesses the first processing circuit and the second processing circuit to which common supply voltage is supplied, and is an integrated circuit device which operation mode and a standby mode can switch freely as a mode of operation. The first processing circuit possessing the first transistor which gate dielectric film is formed by the predetermined thickness a, and drives only operation mode with the predetermined electrical potential difference A, The second processing circuit possessing the second transistor which gate dielectric film is formed by the predetermined thickness b, and is driven by both operation mode and the standby mode with the predetermined electrical potential difference B is provided, and the relation which said Thickness a and b and said electrical potential differences A and B become a<bA=B is satisfied.

[0014] Therefore, with the integrated circuit device of this invention, the first transistor and the second transistor from which the thickness of gate dielectric film is different drive on the same electrical potential difference A (=B). Since gate dielectric film does not have ****** as for the second transistor, although actuation is a low speed, a standby mode is also driven in the condition with a very small gate leakage current. Since the gate dielectric film of the first transistor is the maximum **, although a gate leakage current is not very small, only operation mode is driven in the condition of operating at a high speed.

[0015] The third integrated circuit device of this invention possesses the first processing circuit and the second processing circuit to which common supply voltage is supplied, and is an integrated circuit device which operation mode and a standby mode can switch freely as a mode of operation. The first processing circuit possessing the first transistor which gate dielectric film is formed by the predetermined thickness a, and drives only operation mode with the predetermined electrical potential difference A, The second processing circuit possessing the second transistor which gate dielectric film is formed by the predetermined thickness b, and is driven by both operation mode and the standby mode with the predetermined electrical potential difference B, The third processing circuit possessing the third transistor which gate dielectric film is formed by the predetermined thickness c, and is driven on the predetermined electrical potential difference C is provided, and the

relation which said thickness a-c and said electrical-potential-difference A-C become a<b<cA=B<C is satisfied.

[0016] Therefore, in the integrated circuit device of this invention, the third transistor is driven on the high-pressure electrical potential difference C, and drives the first transistor and the second transistor on the low-pressure electrical potential difference A (=B). Although driver voltage is high pressure, since gate dielectric film is ** thickness, the third transistor operates at a high speed in the condition with a very small gate leakage current. Although driver voltage is low voltage, since the gate dielectric film of the first transistor is the maximum **, although a gate leakage current is not very small, only operation mode operates at a high speed. Gate dielectric film does not have ****** of the second transistor, and since driver voltage is low voltage, a standby mode also operates at a low speed from the first transistor in the condition with a very small gate leakage current.

[0017] The first processing circuit possessing the first transistor which the fourth integrated circuit device of this invention is formed by the thickness a predetermined in gate dielectric film, and is driven on the predetermined electrical potential difference A, The second processing circuit possessing the second transistor which gate dielectric film is formed by the predetermined thickness b, and is driven on the predetermined electrical potential difference B, The third processing circuit possessing the third transistor which gate dielectric film is formed by the predetermined thickness c, and is driven on the predetermined electrical potential difference C is provided, and the relation which said thickness a-c and said electrical-potential-difference A-C become a<b<cA=B<C is satisfied.

[0018] Therefore, in the integrated circuit device of this invention, the third transistor is driven on the high-pressure electrical potential difference C, and drives the first transistor and the second transistor on the low-pressure electrical potential difference A (=B). Although driver voltage is high pressure, since gate dielectric film is ** thickness, the third transistor operates at a high speed in the condition with a very small gate leakage current. Although driver voltage is low voltage, since the gate dielectric film of the first transistor is the maximum **, although a gate leakage current is not very small, it operates at a high speed. Since driver voltage is low voltage that gate dielectric film does not have ******, the second transistor operates at a low speed from the first transistor in the condition with a very small gate leakage current.

[0019] In the above integrated circuit devices, said second processing circuit is able to control the existence of actuation of said first processing circuit. In this case, the second processing circuit which is also driving the standby mode controls the drive of the first processing circuit.

[0020] In the above integrated circuit devices, said second processing circuit can also start electrical-potential-difference supply in said first processing circuit, if the external input of a Sadanobu Tokoro number is detected to a standby mode. In this case, since electrical-potential-difference supply in the first processing circuit will be started if the second processing circuit of a standby mode detects the external input of a Sadanobu Tokoro number, the first processing circuit of a standby mode is started by the external input of a predetermined signal.

[0021] In the above integrated circuit devices, the gate dielectric film of said second transistor is able for the gate dielectric film of said first transistor to consist of thermal oxidation film which grew up to be the front face of a semi-conductor substrate, and to become the front face of said semi-conductor substrate with which at least one of an argon, fluorine, and the fluorides was poured in from the gate dielectric film of said first transistor, and the thermal oxidation film which grew up to be coincidence.

[0022] In this case, since the thermal oxidation film which grew up to be the front face of the semi-conductor substrate with which at least one of an argon, fluorine, and the fluorides was poured in turns into a thick film from the thermal oxidation film which grew up to be coincidence on the front face which is not poured in, the gate oxide of the second transistor is formed in a thick film from the gate oxide of the first transistor.

[0023] In the above integrated circuit devices, the gate dielectric film of said first transistor is able for the gate dielectric film of said second transistor to consist of thermal oxidation film which grew up to be the front face of a semi-conductor substrate, and to become the front face of said semi-conductor substrate with which at least one side of an indium and nitrogen was poured in from the gate dielectric film of said second transistor, and the thermal oxidation film which grew up to be coincidence.

[0024] In this case, since the thermal oxidation film which grew up to be the front face of the semi-conductor substrate with which at least one side of an indium and nitrogen was poured in turns into a thin film from the thermal oxidation film which grew up to be coincidence on the front face which is not poured in, the gate oxide of the first transistor is formed in a thin film from the gate oxide of the second transistor.

[0025] In the above integrated circuit devices, said supply voltage is able to be supplied from the dc-battery of another object. In this case, the supply voltage which a dc-battery generates is supplied common to the first processing circuit and the second processing circuit.

[0026] The first electronic-circuitry device of this invention possesses the first processing circuit and the second processing circuit to which common supply voltage is supplied, and is an electronic-circuitry device which operation mode and a standby mode can switch freely as a mode of operation. The power source which supplies supply voltage to the second processing circuit for a start [said], and the dc-battery which supplies body power to this power source, The electric power switch which turns on/switches [off] the electric power supply of this dc-battery is provided. As for said second processing circuit, the firm gas of the supply voltage is carried out to the ON state of said electric power switch. Said first processing circuit has the thickness of the gate dielectric film of the second transistor which said second processing circuit possesses thicker than the thickness of the gate dielectric film of the first transistor with which supply of supply voltage is suspended in a standby mode, and said first processing circuit also possesses the ON state of said electric power switch.

[0027] Therefore, by the electronic-circuitry device of this invention, if an electric power switch is turned on, body power will be supplied to a power source from a dc-battery, and although the firm gas of the supply voltage is carried out to the second processing circuit, only operation mode is supplied to the first processing circuit. Since gate dielectric film does not have ****** as for the second transistor, although actuation is a low speed, a standby mode is also driven in the condition with a very small gate leakage current. Since the gate dielectric film of the first transistor is the maximum **, although a gate leakage current is not very small, only operation mode is driven in the condition of operating at a high speed.

[0028] The second electronic-circuitry device of this invention is an electronic-circuitry device which operation mode and a standby mode can switch freely as a mode of operation. The third integrated circuit device of this invention, The low-battery power source which supplies an electrical potential difference A (=B) to the second processing circuit for a start [of this integrated circuit device], the high-voltage power source which supplies an electrical potential difference C to said third processing circuit, and the notice means of data which gives the data notice of the predetermined data which can judge the necessity of actuation of said first processing circuit in said second processing circuit are provided.

[0029] Therefore, by the electronic-circuitry device of this invention, a low-battery power source supplies an electrical potential difference A (=B) to the second processing circuit for a start [of an integrated circuit device], and a high-voltage power source supplies an electrical potential difference C to the third processing circuit. However, since the notice means of data gives the data notice of the predetermined data which can judge the necessity of actuation of the first processing circuit in the second processing circuit, this second processing circuit controls the existence of actuation of the first processing circuit corresponding to the notice of data of the notice means of data.

[0030] The first circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and a resist mask is formed in the location of the third processing circuit for a start [of the front face of this thermal oxidation film / said]. At least one of an argon, fluorine, and the fluorides is poured into said thermal oxidation film of the location of said second processing circuit exposed from this resist mask. Said thermal oxidation film of the location of the second processing circuit is removed for a start [said] after this impregnation. the thermal oxidation film is grown up throughout the front face of said semi-conductor substrate with which the thermal oxidation film grew up to be the location of said third processing circuit, and said impregnation was performed in the location of said second processing circuit -- making -- this thermal oxidation film -- the [said / the first transistor and / said] -- the gate electrode of the 2 third transistor is formed.
[0031] Therefore, by the circuit manufacture approach of this invention, although the thermal oxidation film is formed in the location of the second processing circuit for a start at coincidence, since only the location of the second processing circuit pours in an argon, fluorine, and the fluoric acid-ized film, as for the thermal oxidation film of the location of this second processing circuit, growth is promoted from the location of the first processing circuit. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit.
[0032] The second circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and a resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film of the location of the second processing circuit is removed for a start [said] which has been exposed from this resist mask. A resist mask is formed in the location of said second processing circuit where this thermal oxidation film was removed. At least one side of an indium and nitrogen is injected into said semi-conductor substrate of the location of said first processing circuit exposed from this resist mask. after this impregnation, said resist mask is removed and the thermal oxidation film is grown up throughout the front face of said semi-conductor substrate -- making -- this thermal oxidation film -- the [said / the first transistor and / said] -- the gate electrode of the 2 third transistor was formed.
[0033] Therefore, by the circuit manufacture approach of this invention, although the thermal oxidation film is formed in the location of the second processing circuit for a start at coincidence, since only the location of the first processing circuit pours in an indium and nitrogen, as for the thermal oxidation film of the location of this first processing circuit, growth is reduced from the location of the second processing circuit. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit.
[0034] The third circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the thermal oxidation mask which prevents thermal oxidation is formed in the location of said first processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of said semi-conductor substrate of the location of the 2 third processing circuits. the [which has been exposed from this thermal oxidation mask / said] -- A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film of the location of said second processing circuit exposed from this resist mask and said thermal oxidation mask is removed. the [which removed said resist mask and has been exposed from said thermal oxidation mask after removal of this thermal oxidation film / said] -- the thermal oxidation film is grown up to be the location of the 2 third processing circuits --

making -- said thermal oxidation film -- the [said / the first transistor and / said] -- the gate electrode of the 2 third transistor was formed.
[0035] therefore -- since the location of the first processing circuit grows up the thermal oxidation film into proper thickness by the circuit manufacture approach of this invention -- this -- a thermal oxidation mask -- covering -- the -- since the thermal oxidation film is grown up into the location of the 2 third processing circuits -- the -- the thermal oxidation film of the location of the 1 second processing circuit is formed of thickness original with each. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit.
[0036] The fourth circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the thermal oxidation mask which prevents thermal oxidation is formed in the location of said second processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of said semi-conductor substrate of the location of the third processing circuit for a start [said] which has been exposed from this thermal oxidation mask. A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film of the location of said first processing circuit exposed from this resist mask and said thermal oxidation mask is removed. the [which removed said resist mask and has been exposed from said thermal oxidation mask after removal of this thermal oxidation film / said] -- the thermal oxidation film is grown up to be the location of the 1 third processing circuit -- making -- said thermal oxidation film -- the [said / the first transistor and / said] -- the gate electrode of the 2 third transistor was formed.
[0037] Therefore, by the circuit manufacture approach of this invention, since the location of the second processing circuit grows up the thermal oxidation film into proper thickness, this is covered with a thermal oxidation mask and the thermal oxidation film is grown up into the location of the third processing circuit for a start, the thermal oxidation film of the location of the second processing circuit is respectively formed of original thickness for a start. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit.
[0038] In the above circuit manufacture approaches, it is also possible to form said thermal oxidation mask by the conductive layer, and to form the gate electrode of said first transistor at least by this conductive layer. In this case, the gate electrode of the first transistor is formed from the conductive layer of the thermal oxidation mask formed in order to control the thickness of the gate dielectric film of the first transistor.
[0039] In the above circuit manufacture approaches, it is also possible to form the conductive layer of said thermal oxidation mask by the polish recon film. In this case, the polish recon film can prevent lower layer thermal oxidation good in physical properties, and can use it as conductive layers, such as a gate electrode.
[0040] The fifth circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said first processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. the [which has been exposed / said] -- A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said second processing circuit exposed from this resist mask, and said first polish recon film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. after removal of this thermal oxidation film

-- said resist mask -- removing -- the [said] -- The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. A resist mask is formed in the location of the 2 third processing circuits. the [of the front face of this second polish recon film / said] -- Said second polish recon film of the location of said first processing circuit exposed from this resist mask is removed. Remove said thermal oxidation film of the location of said first processing circuit exposed by this removal, and said first polish recon film is exposed. Said resist mask is removed from the location of the 2 third processing circuits, and said second polish recon film is exposed. the [said] -- While carrying out patterning of said first polish recon film of the location of said first processing circuit and forming the gate electrode of said first transistor the [said] -- said second polish recon film of the location of the 2 third processing circuits -- patterning -- carrying out -- the [said] -- the gate electrode of the 2 third transistor was formed.
[0041] therefore -- since the location of the first processing circuit grows up the thermal oxidation film into proper thickness by the circuit manufacture approach of this invention -- this -- the first polish recon film -- covering -- the -- since the thermal oxidation film is grown up into the location of the 2 third processing circuits -- the -- the thermal oxidation film of the location of the 1 second processing circuit is formed of thickness original with each. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit. And the gate electrode of the first transistor is formed from the first polish recon film formed in order to control the thickness of the gate dielectric film of the first transistor.
[0042] The sixth circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said second processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said] which has been exposed. A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said first processing circuit exposed from this resist mask, and said first polish recon film. Remove said resist mask after removal of this thermal oxidation film, and the thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said]. The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. A resist mask is formed in the location of the third processing circuit for a start [of the front face of this second polish recon film / said]. Said second polish recon film of the location of said second processing circuit exposed from this resist mask is removed. Remove said thermal oxidation film of the location of said second processing circuit exposed by this removal, and said first polish recon film is exposed. Remove said resist mask from the location of the third processing circuit for a start [said], and said second polish recon film is exposed. While carrying out patterning of said first polish recon film of the location of said second processing circuit and forming the gate electrode of said second transistor Patterning of said second polish recon film of the location of the third processing circuit is carried out for a start [said], and the gate electrode of the third transistor was formed for a start [said].
[0043] Therefore, by the circuit manufacture approach of this invention, since the location of the second processing circuit grows up the thermal oxidation film into proper thickness, this is covered by the first polish recon film and the thermal oxidation film is grown up into the location of the third processing circuit for a start, the thermal oxidation film of the location of the second processing circuit is respectively formed of original thickness for a start. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit. And the gate electrode of the second transistor is formed from the first polish recon film formed in order to control the thickness of the gate dielectric film of

the second transistor.

[0044] The seventh circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said first processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. the [which has been exposed / said] -- A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said second processing circuit exposed from this resist mask, and said first polish recon film. The thermal oxidation film is grown up into the front face of the location of the 2 third processing circuits, and said first polish recon film. after removal of this thermal oxidation film -- said resist mask -- removing -- the [said] -- The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. The gate electrode of the 2 third transistor is formed. while removing this second polish recon film from the location of said first processing circuit -- the [said] -- the location of the 2 third processing circuits -- patterning -- carrying out -- the [said] -- the [said] -- the resist mask was formed in the location of the 2 third processing circuits, patterning of said first polish recon film of the location of said first processing circuit exposed from this resist mask is carried out, and the gate electrode of said first transistor was formed.

[0045] therefore -- since the location of the first processing circuit grows up the thermal oxidation film into proper thickness by the circuit manufacture approach of this invention -- this -- the first polish recon film -- covering -- the -- since the thermal oxidation film is grown up into the location of the 2 third processing circuits -- the -- the thermal oxidation film of the location of the 1 second processing circuit is formed of thickness original with each. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit. And the gate electrode of the first transistor is formed from the first polish recon film formed in order to control the thickness of the gate dielectric film of the first transistor. furthermore, etching of the gate electrode located in the front face of the gate oxide of the maximum ** of the first transistor -- the -- it performs separately from etching of the gate electrode of the 2 third transistor.

[0046] The eighth circuit manufacture approach of this invention is the circuit manufacture approach of manufacturing the first of this invention, or the third integrated circuit device. Grow up the thermal oxidation film throughout the front face of a semi-conductor substrate, and the first polish recon film which prevents thermal oxidation is formed in the location of said second processing circuit of the front face of this thermal oxidation film. The thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said] which has been exposed. A resist mask is formed in the location of said third processing circuit of the front face of this thermal oxidation film. Said thermal oxidation film is removed from the front face of the location of said first processing circuit exposed from this resist mask, and said first polish recon film. Remove said resist mask after removal of this thermal oxidation film, and the thermal oxidation film is grown up into the front face of the location of the third processing circuit, and said first polish recon film for a start [said]. The second polish recon film is formed in the front face of this thermal oxidation film and said first polish recon film. While removing this second polish recon film from the location of said second processing circuit, carry out patterning for a start [said] in the location of the third processing circuit, and the gate electrode of the third transistor is formed for a start [said]. The resist mask was formed in the location of the third processing circuit for a start [said], patterning of said first polish recon film of the location of said second processing circuit exposed from this resist mask is carried out, and the gate electrode of said second transistor was formed.

[0047] Therefore, by the circuit manufacture approach of this invention, since the location of the second processing circuit grows up the thermal oxidation film into proper thickness, this is covered by the first polish recon film and the thermal oxidation film is grown up into the location of the third processing circuit for a start, the thermal oxidation film of the location of the second processing circuit is respectively formed of original thickness for a start. Since the thermal oxidation film consists of a bilayer, the location of the third processing circuit is formed in a thick film from the location of the second processing circuit. And the gate electrode of the second transistor is formed from the first polish recon film formed in order to control the thickness of the gate dielectric film of the second transistor. Furthermore, etching of the gate electrode located in the front face of the gate oxide of the maximum ** of the second transistor is performed separately from etching of the gate electrode of the third transistor for a start.
[0048] In addition, the various means as used in the field of this invention permit the hardware of dedication, the computer by which the proper function was given by the program, the functions realized inside the computer by the proper program, such combination, and ** that what is necessary is to just be formed so that the function may be realized.
[0049]
[Embodiment of the Invention] The first integrated circuit device and circuit manufacture approach of a gestalt of operation of this invention are explained below with reference to drawing 1 thru/or drawing 4 . in addition, process drawing in which the sectional view in which drawing 1 shows the internal structure of the important section of the integrated circuit device of the gestalt of this operation, the typical block diagram in which drawing 2 shows the whole integrated circuit device structure, drawing 3 , and drawing 4 show the circuit manufacture approach of the gestalt this operation -- it comes out.
[0050] The integrated circuit device 100 of the gestalt of this operation is formed as some portable telephones (not shown) which are electronic-circuitry devices, and this portable telephone possesses the low-battery power source 101, the high-voltage power source 102, a dc-battery, an electric power switch, various kinds of external components (not shown), etc. with the integrated circuit device 100.
[0051] The body of equipment is equipped with the dc-battery free [attachment and detachment], and it supplies body power to each power source 101,102. The electric power switch is prepared in the condition that it can operate manually on the external surface of the body of equipment, and turns on/switches [off] the electric power supply from the dc-battery to each power source 101,102. The low-battery power source 101 generates the low battery A (=B) of 1.2 (V) with the body power supplied from a dc-battery, and the high-voltage power source 102 generates the high voltage C of 3.3 (V).
[0052] The integrated circuit device 100 of the gestalt of this operation possesses the three first processing circuits 111, the second processing circuit 112 of a piece, and the I/O (Input/Output) circuit 113 of the piece which is the third processing circuit, and these are connected mutually. The low-battery power source 101 is connected to the first processing circuit 111 and the second processing circuit 112, and the high-voltage power source 102 and various kinds of external components are connected to the I/O circuit 113.
[0053] Since the integrated circuit device 100 of the gestalt of this operation is formed as some portable telephones as mentioned above, operation mode and a standby mode are set up as a mode of operation which can be switched freely. Although, as for an integrated circuit device 100, supply voltage is supplied to all parts under a setup in operation mode, as for supply voltage, only some parts are supplied under a setup of a standby mode.
[0054] Then, the I/O circuit 113 is always driven by both operation mode and the standby mode with the high voltage C of 3.3 (V) supplied from the high-voltage power source 102, and outputs and inputs various kinds of external component and various data. The second processing circuit 112 is always driven by both operation mode and the standby mode with the low battery B of 1.2 (V)

supplied from the low-battery power source 101, and by controlling electrical-potential-difference supply in the first processing circuit 111, it is worked at the time of operation mode while stopping the first processing circuit 111 at the time of a standby mode.
[0055] Thus, the first processing circuit 111 where it operates by control of the second processing circuit 112 only at the time of operation mode is driven by the low battery A (=B) of 1.2 (V) supplied from the low-battery power source 101 at the time of the actuation, and the I/O circuit 113 performs various processings corresponding to the exterior, the data which are delivered and received.
[0056] As the first processing circuit 111, the second processing circuit 112, and the I/O circuit 113 are formed in the semi-conductor substrate 120 of the piece made from silicon and are shown in drawing 1 , a part of circuit element [at least] of various kinds [circuit / 111 / first processing] consists of many first transistor 121. Similarly, a part of circuit element [at least] of various kinds [circuit / 112 / second processing] consists of many second transistor 122, and the I/O circuit 113 consists of many third transistor 123.
[0057] These firsts to the third transistor 121-123 is formed by MOSFET (Metal Oxide Semiconductor Field Effect Transistor) of the LDD (Lightly Doped Drain-source) structure respectively formed in the semi-conductor substrate 120 of a piece with the gestalt of this operation, and it dissociates mutually in the trench section 125 as occasion demands.
[0058] In addition, 126 in drawing shows high-concentration source / drain field section, and 127 shows a low concentration field. moreover, the gate dielectric film with which 130 consists of thermal oxidation film, the gate electrode with which 131 consists of polish recon film, and the sidewall which 132 becomes from an oxide film -- it comes out.
[0059] Although the third transistor 121-123 is formed in the same structure from the first as mentioned above, that thickness a-c of gate dielectric film 130 of each has satisfied the relation it is unrelated a<b<c.
[0060] More, the thickness a of the gate dielectric film 130 of the first transistor 121 is 20 (A) at a detail, the thickness b of the gate dielectric film 130 of the second transistor 122 is 24 (A), and the thickness c of the gate dielectric film 130 of the third transistor 123 is 70 (A).
[0061] In addition, although the thickness a of the gate dielectric film 130 of the first transistor 121 is [that what is necessary is just below 21 (A)] so good that it is thin for improvement in the speed of operation, if not much thin, in order that a problem may appear in the dependability in a long period of time, the homogeneity of thickness, etc., it is referred to as 20 (A) as mentioned above.
[0062] Moreover, although the thickness b of the gate dielectric film 130 of the second transistor 122 should be [more than 2.0 (A)] just thicker than Thickness a in 22-28 (A), since a gate leakage current becomes small enough from off-leak (drain current in case the potential difference between a gate electrode and a substrate is "0") and the contribution of a gate leakage current to the consumed electric current at the time of standby can be disregarded if it is above-mentioned thickness, it is referred to as 24 (A).
[0063] Furthermore, since the 3.3(V) thing high voltage is impressed, in order to secure the dependability in a long period of time, it is necessary to be more than 40 (A), and although it is so good that the thickness c of the gate dielectric film 130 of the third transistor 123 is thin for improvement in the speed of operation, it is referred to as 70 (A) in order to secure sufficient dependability here.
[0064] In addition, as mentioned above, since the first processing circuit 111 drives only operation mode by the low battery A of 1.2 (V), the second processing circuit 112 also drives a standby mode by the low battery B (=A) of 1.2 (V) and a standby mode also drives the I/O circuit 113 by the high voltage C of 3.3 (V), electrical-potential-difference A-C which drives the third transistor 121-123 from the first has satisfied the relation it is unrelated A=B<C.
[0065] In the above configurations, since the integrated circuit device 100 of the gestalt of this operation is formed as some portable telephones which are electronic-circuitry devices,

corresponding to the data which the I/O circuit 113 outputs and inputs various kinds of external component and various data, and this I/O circuit 113 outputs and inputs with the exterior, the first processing circuit 111 performs various processings.

[0066] Operation mode and a standby mode can switch the portable telephone of the gestalt of this operation freely as a mode of operation as mentioned above, as usual, operation mode is set up at the time of dispatch and arrival, and it operates at it. However, since a standby mode is set up and it stands by when other, the drive of most circuits is stopped waiting and unnecessary power consumption is prevented. However, since it is necessary to operate immediately if a message is received also waiting, this circuit that arrival of the mail is detected [circuit] also waiting and starts the circuit under pause is operating.

[0067] Then, since the portable telephone of the gestalt of this operation possesses the notice circuit of data (not shown) which is a notice means of data and gives the data notice of the predetermined data with which this notice circuit of data can judge the necessity of actuation of the first processing circuit 111 in the second processing circuit 112, electrical-potential-difference supply in the first processing circuit 111 is controlled by this second processing circuit 112, and existence of operation is controlled.

[0068] For this reason, although the I/O circuit 113 and the second processing circuit 112 are always driven regardless of the mode of operation of a portable telephone, since, as for the first processing circuit 111, an electric power supply is intercepted by the standby mode of a portable telephone, unnecessary power is not consumed by the first processing circuit 111 waiting.

[0069] Although the first processing circuit 111, the second processing circuit 112, and the I/O circuit 113 are accumulated by the semi-conductor substrate 120 of a piece, since the third transistor 121-123 is optimized from the first corresponding to an application or the engine performance, as for the integrated circuit device 100 of the gestalt of this operation, high-performance-izing and power-saving are compatible.

[0070] That is, in order to deliver and receive the I/O circuit 113 with external components, such as a memory device which operates with the supply voltage of 3.3 (V), the high pressure 3.3 (V) supply voltage C always needs to be impressed, but since Thickness c is 70 (A) and ** thickness, as for the gate dielectric film 130 of the third transistor 123, it can operate in the condition with a very small gate leakage current.

[0071] Since the thickness a of the gate dielectric film 130 of the first transistor 121 is 20 (A) and the maximum **, the first processing circuit 111 can operate to a high speed and power saving by the low battery A of 1.2 (V). Thus, although the first transistor 121 of the maximum ** cannot disregard a gate leakage current with waiting gate dielectric film 130, since supply voltage is not impressed waiting, a gate leakage current does not generate the first processing circuit 111.

[0072] and the second processing circuit 112 -- the thickness b of the gate dielectric film 130 of the second transistor 122 -- Thickness a -- a number (A) -- since it is thick 24 (A), the gate leakage current when driving by the low battery B of 1.2 (V) is very small. Thus, since the second processing circuit 112 where a gate leakage current is very small controls electrical-potential-difference supply in the first processing circuit 111 which is always operating also waiting [a portable telephone] and cannot disregard a gate leakage current, power consumption with the total integrated circuit device 100 of the gestalt of this operation is reduced.

[0073] In addition, in the first about 121 transistor of the maximum ** of the second transistor 122 which gate dielectric film 130 drives by the low battery thickly as mentioned above, although gate dielectric film 130 cannot operate at a high speed, since it operates waiting, there is nothing for which, as for the second processing circuit 112, high-speed operation is not demanded and to which the working speed of the second transistor 122 poses a problem.

[0074] The circuit manufacture approach of manufacturing the integrated circuit device 100 of the gestalt of this operation here is explained below. First, the semi-conductor substrate 120 is prepared, and as shown in drawing 3 (a), after forming the trench section 125 in the location which

separates the third transistor 121-123 from the first, the thermal oxidation film 141 of thickness 65 (A) is grown up by the method of oxidizing 850 (degree C) thermally throughout the front face of the semi-conductor substrate 120.
[0075] Next, by removing only the location of the second processing circuit 112 by the photolithography method, after applying a photoresist throughout the front face of this thermal oxidation film 141, as shown in this drawing (b), the resist mask 142 is formed in the location of the first processing circuit 111 of the front face of the thermal oxidation film 141, and the I/O circuit 113.
[0076] Since only the location of the second processing circuit 112 is exposing the thermal oxidation film 141, this resist mask 142 pours argon ion into this exposed thermal oxidation film 141 of the location of the second processing circuit 112 to a dose 5x1014 (/cm2) by reinforcement 20 (KeV).
[0077] After removing the resist mask 142 after impregnation of this argon ion, as shown in this drawing (c), only the location of the I/O circuit 113 forms the resist mask 143 again, and an etching reagent removes the thermal oxidation film 141 of the location of the second processing circuit 111,112 for a start which has been exposed from this resist mask 143. Since the thermal oxidation film 141 has received the damage with argon ion, this is for removing once and forming membranes again.
[0078] Next, after removing the resist mask 143, as the whole region of the front face of the semi-conductor substrate 120 is heat-treated to 10 (sec) by 1000 (degree C) and is shown in drawing 4 (a), one thermal oxidation film 144 is grown up throughout the front face of the semi-conductor substrate 120. Thus, the thermal oxidation film 144 grown up serves as thickness of 20 (A) in the location of the first processing circuit 111.
[0079] However, in the location of the second processing circuit 112, since the argon is poured in, an early oxidation rate improves, and in the thickness of the thermal oxidation film 144, a number (A) becomes 24 (A) of a thick film from the location of the first processing circuit 111. Moreover, in the location of the I/O circuit 113, since the thermal oxidation film 141 is formed in advance, the thickness of the thermal oxidation film 144 becomes 70 (A).
[0080] The following is the same as that of the conventional circuit manufacture approach, as shown in this drawing (b), the gate electrode 131 is formed by forming and carrying out patterning of the polish recon film throughout the front face of the thermal oxidation film 144, and low-concentration n mold diffusion layer 126 is partially formed by the ion implantation restricted with the mask.
[0081] Furthermore, by carrying out etchback, forming a sidewall 132, since the oxide film of 800 (A) is grown up into the whole surface, forming high-concentration n mold diffusion layer 127 by the ion implantation for the second time, and forming an interlayer film, a contact hole, wiring, etc. as occasion demands, as shown in this drawing (c), the third transistor 121-123 is completed from the first of an integrated circuit device 100.
[0082] The integrated circuit device 100 manufactured by the above circuit manufacture approaches has satisfied from the first the relation which thickness a-c of the gate dielectric film 130 of the third transistor 121-123 becomes a<b<c.
[0083] for this reason, in the integrated circuit device 100 of the gestalt of this operation Thickness c the gate dielectric film 130 of the third transistor 123 the I/O circuit 113 of 70 (A) and ** thickness It can operate at a high speed in the condition with a very small gate leakage current with the high voltage C of 3.3 (V), and, as for the first processing circuit 111 of 20 (A) and the maximum **, the thickness a of the gate dielectric film 130 of the first transistor 121 can operate to a high speed and power saving by the low battery A of 1.2 (V).
[0084] the thickness b of the gate dielectric film 130 of the second transistor 122 -- Thickness a -- a number (A) -- the thick second processing circuit 112 of 24 (A) can operate in the condition with a very small gate leakage current with the low battery B of 1.2 (V). Although the second processing circuit 112 cannot operate at a high speed the about 111 first processing circuit, since

the second processing circuit 112 operates waiting, a rate does not pose a problem. Although the first processing circuit 111 does not have a very small gate leakage current, since control of the second processing circuit 112 stops waiting and an electrical potential difference is not supplied, the gate leakage current is not consumed unnecessarily.

[0085] That is, since the transistors 121-123 of the first processing circuit 111 and the second processing circuit 112 on which the integrated circuit device 100 of the gestalt of this operation is accumulated by the semi-conductor substrate 120 of a piece, and the I/O circuit 113 are optimized corresponding to an application or the engine performance, high-performance-izing and power-saving are compatible.

[0086] In addition, this invention is not limited to the above-mentioned gestalt, and permits various kinds of deformation in the range which does not deviate from the summary. For example, although it illustrated using each transistors 121-123 as n mold of a LDD format with the above-mentioned gestalt, naturally an anhedron type is also possible.

[0087] Moreover, although it illustrated always operating the I/O circuit 113 which is the third processing circuit by both operation mode and the standby mode with the above-mentioned gestalt, it is also possible to make a standby mode stop the electric power supply of the I/O circuit 113 by the first processing circuit 112, and to reduce power consumption further.

[0088] Furthermore, although the portable telephone was illustrated with the above-mentioned gestalt as an electronic-circuitry device which operation mode and a standby mode can switch freely, this invention is applicable to various kinds of electronic-circuitry devices which carry out a dc-battery drive, such as a notebook computer. Moreover, although various kinds of numeric values were concretely illustrated with the above-mentioned gestalt, as for this, it is natural that it can change into various kinds with an actual product.

[0089] Moreover, although it illustrated that only the location of the second processing circuit 112 carried out the ion implantation of the argon with the above-mentioned gestalt in order to use as a thick film the gate dielectric film 130 of the second transistor 122 grown up into coincidence by the oxidizing [thermally] method from the gate dielectric film 130 of the first transistor 121, it is also possible to make into fluorine or a fluoride this matter that carries out an ion implantation.

[0090] Since the gate dielectric film 130 of the first transistor 121 grown up into coincidence by the oxidizing [thermally] method is used as a thin film on the contrary than the gate dielectric film 130 of the second transistor 122, it is also possible to pour in the matter which reduces growth of the thermal oxidation film in the location of the first processing circuit 111.

[0091] Here, such a circuit manufacture approach is explained below with reference to drawing 5 and drawing 6 as the second gestalt of operation of this invention. In addition, detailed explanation is omitted using a name and a sign with the same, same part as the first gestalt mentioned above in the gestalt of the following operations from this. This drawing is process drawing showing the circuit manufacture approach of the gestalt this operation.

[0092] First, as shown in drawing 5 (a), after forming the trench section 125 in the location which separates the third transistor 121-123 from the first of the semi-conductor substrate 120 also by the circuit manufacture approach of the gestalt this operation, the thermal oxidation film 141 of thickness 5.0 (nm) is grown up by the oxidizing [thermally] method throughout the front face of the semi-conductor substrate 120.

[0093] Next, by removing only the location of the second processing circuit 111,112 by the photolithography method for a start, after applying a photoresist throughout the front face of this thermal oxidation film 141, as shown in this drawing (b), only the location of the I/O circuit 113 of the front face of the thermal oxidation film 141 forms the resist mask 151.

[0094] This resist mask 151 forms the resist mask 152 in the location of the second processing circuit 112 and the I/O circuit 113 again, after removing the thermal oxidation film 141 of the location of the second processing circuit 111,112 by wet etching for a start [this] that has been exposed, since only the location of the second processing circuit 111,112 exposes the thermal

oxidation film 141 for a start.
[0095] Since only the location of the first processing circuit 111 exposes the thermal oxidation film 141, this resist mask 152 pours indium ion (In+) into this exposed thermal oxidation film 141 of the location of the first processing circuit 111 by reinforcement 100-300 (KeV) to a dose "1x1012 to 3x1013 (/cm2)."
[0096] After impregnation of this indium ion, as shown in this drawing (c), only the location of the first processing circuit 111 and the I/O circuit 113 forms the resist mask 153 again, and boron ion (B+) is poured into the thermal oxidation film 141 of the location of the second processing circuit 112 exposed from this resist mask 153 by reinforcement 10-50 (KeV) to a dose "1x1012 to 3x1013 (/cm2)."
[0097] Next, after removing the resist mask 153, one thermal oxidation film 144 is grown up throughout the front face of the semi-conductor substrate 120, and this thermal oxidation film 144 is set to 25 (A) in the location of the second processing circuit 112. At this time, since the indium is poured in, an early oxidation rate is reduced, and in the thickness of the thermal oxidation film 144, a number (A) becomes 20 (A) of a thin film from the location of the second processing circuit 112 in the location of the first processing circuit 111. Moreover, in the location of the I/O circuit 113, since the thermal oxidation film 141 is formed in advance, the thickness of the thermal oxidation film 144 becomes 70 (A).
[0098] The integrated circuit device 100 which that of the following is the same as that of the conventional circuit manufacture approach, and was manufactured by the above circuit manufacture approaches will satisfy from the first the relation which thickness a-c of the gate dielectric film 130 of the third transistor 121-123 becomes a<b<c.
[0099] In addition, since, as for the first transistor 121, the ion implantation of the indium is carried out to gate oxide 130, threshold voltage is also controlled proper with the thickness. Moreover, although the ion implantation of the boron is carried out to the gate oxide 130 of the second transistor 122, this is for controlling threshold voltage and does not participate in control of thickness.
[0100] Moreover, although it illustrated that only the location of the first processing circuit 111 carried out the ion implantation of the indium with the above-mentioned gestalt in order to grow up into a thin film the gate dielectric film 130 of the first transistor 121 grown up into coincidence by the oxidizing [thermally] method from the gate dielectric film 130 of the second transistor 122, it is also possible to use as nitrogen this matter that carries out an ion implantation.
[0101] Furthermore, the circuit manufacture approach of the third gestalt operation of this invention is explained below with reference to drawing 7 thru/or drawing 9 . In addition, this drawing is process drawing showing the circuit manufacture approach of the gestalt this operation. First, also by the circuit manufacture approach of the gestalt this operation, as shown in drawing 7 (a), after forming the trench section 125 in the location which separates the third transistor 121-123 from the first of the semi-conductor substrate 120, the thermal oxidation film 141 is grown up throughout a front face, and the first polish recon film 161 is formed as a conductive layer throughout the front face of this thermal oxidation film 141.
[0102] Next, as shown in this drawing (b), the resist mask 162 is formed in the location of the first processing circuit 111 of the front face of this first polish recon film 161, and only the location of the second processing circuit 112 and the I/O circuit 113 which have been exposed from this resist mask 162 removes the first polish recon film 161.
[0103] Now, since the first polish recon film 161 is formed as a thermal oxidation mask, only the location of the first processing circuit 111 grows up the thermal oxidation film 163 into the front face of the location of the second processing circuit 112 and the I/O circuit 113, after removing the resist mask 162, as shown in this drawing (c). At this time, this thermal oxidation film 163 is formed also in the front face of the first polish recon film 161, and is united with the lower layer thermal oxidation film 141 of this first polish recon film 161.

[0104] Next, the resist mask 164 is formed in the location of the I/O circuit 113 of the front face of this thermal oxidation film 163, and as shown in drawing 8 (a), etching removal of the thermal oxidation film 163 is carried out from the front face of the location of the second processing circuit 112 and the first polish recon film 161 which have been exposed from this resist mask 164.
[0105] The resist mask 164 is removed after removal of this thermal oxidation film 163, and as shown in this drawing (b), the thermal oxidation film 144 is grown up throughout the location of the second processing circuit 112 and the I/O circuit 113, and the front face of the first polish recon film 161. Thickness a-c of the thermal oxidation film 144 of the location of the first processing circuit 111, the second processing circuit 112, and the I/O circuit 113 serves as "a<b<c" now.
[0106] Furthermore, by the circuit manufacture approach of the gestalt this operation, as shown in this drawing (c), the second polish recon film 166 is formed as a conductive layer throughout the front face of the thermal oxidation film 144 formed as mentioned above, and the resist mask 167 is formed in the location of the second processing circuit 112 of the front face of this second polish recon film 166, and the I/O circuit 113.
[0107] As shown in drawing 9 (a), the second polish recon film 166 of the location of the first processing circuit 111 exposed from this resist mask 167 is removed by anisotropic etching, and wet etching removes the thermal oxidation film 144 of the location of the first processing circuit 111 exposed by this removal.
[0108] Since the first polish recon film 161 is exposed now, as shown in this drawing (b), the resist mask 167 is removed from the location of the second processing circuit 112 and the I/O circuit 113, the second polish recon film 166 is also exposed, and the resist mask 168 of the configuration of the gate electrode 131 is formed in the front face of the second polish recon film 161,166 for a start [these].
[0109] And while carrying out patterning of the first polish recon film 161 of the location of the first processing circuit 111 with this resist mask 168, the gate electrode 131 of the third transistor 121-123 is formed in coincidence from the first by carrying out patterning of the second polish recon film 166 of the location of the second processing circuit 112 and the I/O circuit 113.
[0110] By the circuit manufacture approach of the gestalt this operation, thickness a-c of the gate dielectric film 130 of the third transistor 121-123 can be made into "a<b<c" from the first by forming the first polish recon film 161 as a thermal oxidation mask, without needing an ion implantation.
[0111] And since the gate electrode 131 of the first transistor 121 can be formed from the first polish recon film 161 used in order to control the thickness of the gate dielectric film 130 of the third transistor 121-123 from the first in this way, the productivity of an integrated circuit device 100 can be raised.
[0112] Furthermore, the circuit manufacture approach of the fourth gestalt operation of this invention is explained below with reference to drawing 10 thru/or drawing 12 . First, although the thermal oxidation film 141 and the first polish recon film 161 are formed in order throughout a front face also by the circuit manufacture approach of the gestalt this operation after forming the trench section 125 in the semi-conductor substrate 120 as shown in drawing 10 (a) As shown in this drawing (b), the resist mask 162 is formed in the location of the second processing circuit 112 of the front face of this first polish recon film 161, and only the location of the first processing circuit 111 and the I/O circuit 113 removes the first polish recon film 161.
[0113] Now, since the first polish recon film 161 is formed as a thermal oxidation mask, only the location of the second processing circuit 112 grows up the thermal oxidation film 163 into the location of the first processing circuit 111 and the I/O circuit 113, and the front face of the first polish recon film 161, after removing the resist mask 162, as shown in this drawing (c).
[0114] Next, the resist mask 164 is formed in the location of the I/O circuit 113 of the front face of this thermal oxidation film 163, and as shown in drawing 11 (a), etching removal of the thermal oxidation film 163 is carried out from the front face of the location of the first processing circuit 111

and the first polish recon film 161 which have been exposed from this resist mask 164.
[0115] The resist mask 164 is removed after removal of this thermal oxidation film 163, and as shown in this drawing (b), the thermal oxidation film 144 is grown up throughout the location of the first processing circuit 111 and the I/O circuit 113, and the front face of the first polish recon film 161. Thickness a-c of the thermal oxidation film 144 of the location of the first processing circuit 111, the second processing circuit 112, and the I/O circuit 113 serves as "a<b<c" now.
[0116] Furthermore, by the circuit manufacture approach of the gestalt this operation, as shown in this drawing (c), the second polish recon film 166 is formed throughout the front face of the thermal oxidation film 144 formed as mentioned above, and the resist mask 167 is formed in the location of the first processing circuit 111 of the front face of this second polish recon film 166, and the I/O circuit 113.
[0117] As shown in drawing 12 (a), the second polish recon film 166 of the location of the second processing circuit 112 exposed from this resist mask 167 is removed by anisotropic etching, and wet etching removes the thermal oxidation film 144 of the location of the second processing circuit 112 exposed by this removal.
[0118] Since the first polish recon film 161 is exposed now, as shown in this drawing (b), the gate electrode 131 of the third transistor 121-123 is formed in coincidence from the first by removing the resist mask 167 from the location of the first processing circuit 111 and the I/O circuit 113, also exposing the second polish recon film 166, and carrying out patterning of the second polish recon film 161,166 for a start [these].
[0119] Also by the circuit manufacture approach of the gestalt this operation, by forming the first polish recon film 161 as a thermal oxidation mask, thickness a-c of the gate dielectric film 130 of the third transistor 121-123 can be made into "a<b<c" from the first, without needing an ion implantation, and the gate electrode 131 of the second transistor 122 can be formed from the first polish recon film 161.
[0120] Furthermore, the circuit manufacture approach of the fifth gestalt operation of this invention is explained below with reference to drawing 13 and drawing 14 . First, by the circuit manufacture approach of the gestalt this operation as well as the third gestalt mentioned above, as shown in drawing 13 (a) The thermal oxidation film 144 of "a<b<c" is formed in the front face of the semi-conductor substrate 120 for thickness a-c of the location of the first processing circuit 111, the second processing circuit 112, and the I/O circuit 113. While the first polish recon film 161 is formed in the location of the first processing circuit 111, it considers as the condition that the second polish recon film 166 is formed throughout the front face.
[0121] from such a condition, it is shown in this drawing (b) -- as -- the front face of the second polish recon film 166 -- the, as the resist mask 171 of the configuration of the gate electrode 131 of the 2 third transistor 122,123 is formed and it is shown in this drawing (c) the anisotropic etching using this resist mask 171 -- the second polish recon film 166 -- the location of the second processing circuit 112 and the I/O circuit 113 -- patterning -- carrying out -- the -- the gate electrode 131 of the 2 third transistor 122,123 is formed.
[0122] Although the second polish recon film 166 is removed from the location of the first processing circuit 111 at this time, since the thermal oxidation film of the first polish recon film 161 is located as a lower layer of the second polish recon film 166 in the location of this first processing circuit 111, anisotropic etching is suspended by this thermal oxidation film.
[0123] Next, while covering the location of the second processing circuit 112 and the I/O circuit 113, the resist mask 172 corresponding to the configuration of the gate electrode 131 of the first transistor 121 is formed, patterning of the first polish recon film 161 of the location of the first processing circuit 111 exposed from this resist mask 172 is carried out, and the gate electrode 131 of the first transistor 121 is formed.
[0124] And if the resist mask 172 is removed after this formation, as shown in this drawing (b), thickness a-c of the location of the first processing circuit 111, the second processing circuit 112,

and the I/O circuit 113 will be in the condition that the gate electrode 131 of the third transistor 121-123 was formed in the front face of the thermal oxidation film 144 of "a<b<c" from the first.
[0125] etching of the gate electrode 131 located in the front face of the gate oxide 130 of the maximum ** of the first transistor 121 by the circuit manufacture approach of the gestalt this operation -- the -- it is performing separately from etching of the gate electrode 131 of the 2 third transistor 122,123.
[0126] for this reason, the thickness of the gate oxide 130 of the first transistor 121 -- the -- even when thinner to the degree of pole than the 2 third transistor 122,123, it is possible to etch the gate electrode 131 of the third transistor 121-123 on the optimal conditions for each from the first.
[0127] In addition, while the thermal oxidation film 144 of thickness a-c of "a<b<c" is formed in the front face of the semi-conductor substrate 120 like the fourth gestalt which mentioned such a circuit manufacture approach above and the first polish recon film 161 is formed in the location of the second processing circuit 112, it is also possible to apply to the condition that the second polish recon film 166 is formed throughout the front face.
[0128] In that case, as shown in drawing 15 and drawing 16 , since etching of the gate electrode 131 located in the front face of the gate oxide 130 of the second transistor 122 is performed separately from etching of the gate electrode 131 of the third transistor 121,123 for a start, it becomes possible [etching the gate electrode 131 of the third transistor 121-123 on the optimal conditions for each] from the first too.
[0129]
[Effect of the Invention] Since this invention is constituted as explained above, effectiveness which is indicated below is done so.
[0130] With the second integrated circuit device, gate dielectric film drives for a start [of this invention] on an electrical potential difference with same first transistor of a thin film and second transistor of a thick film. Although actuation is a low speed since gate dielectric film does not have ****** as for the second transistor when the first transistor drives only operation mode although a standby mode also drives the second transistor It can always operate in the condition with a very small gate leakage current. The first transistor Since only operation mode is driven in the condition of operating at a high speed although a gate leakage current is not very small since gate dielectric film is the maximum ** and the second transistor is optimized for a start corresponding to an application or the engine performance, high-performance-izing and power-saving are compatible.
[0131] In the third integrated circuit device of this invention, gate dielectric film drives the third transistor of ** thickness by the high voltage. Although the second transistor in which the first transistor and ****** of the maximum ** do not have gate dielectric film is driven by the low battery and a standby mode also drives the second transistor, the first transistor by driving only operation mode Although driver voltage is high pressure, since gate dielectric film is ** thickness, the third transistor can operate at a high speed in the condition with a very small gate leakage current. The second transistor Since driver voltage is low voltage that gate dielectric film does not have ******, it can always operate at a low speed in the condition with a very small gate leakage current. The first transistor Although driver voltage is low voltage, since gate dielectric film is the maximum **, although a gate leakage current is not very small, since only operation mode can operate at a high speed and the third transistor is optimized from the first corresponding to an application or the engine performance, high-performance-izing and power-saving are compatible.
[0132] By gate dielectric film's driving the third transistor of ** thickness by the high voltage, and driving the second transistor in which the first transistor and ****** of the maximum ** do not have gate dielectric film by the low battery in the fourth integrated circuit device of this invention Although driver voltage is high pressure, since gate dielectric film is ** thickness, the third transistor can operate at a high speed in the condition with a very small gate leakage current. The second transistor Since driver voltage is low voltage that gate dielectric film does not have ******, it can operate at a low speed in the condition with a very small gate leakage current. The first

transistor Although driver voltage is low voltage, since gate dielectric film is the maximum **, although a gate leakage current is not very small, since it can operate at a high speed and the third transistor is optimized from the first corresponding to an application or the engine performance, high-performance-izing and power-saving are compatible.

[0133] Moreover, in the above integrated circuit devices, although actuation is a low speed, since it can operate at a high speed when the second processing circuit always driven controls the drive of the first processing circuit, but the second processing circuit where a gate leakage current is very small controls the existence of the actuation of the first processing circuit whose gate leakage current at the time of standby is not very small, it is compatible in high-performance-izing and power-saving.

[0134] Moreover, if the second processing circuit of a standby mode detects the external input of a Sadanobu Tokoro number, the first processing circuit of a standby mode can be started by the external input of a predetermined signal by starting electrical-potential-difference supply in the first processing circuit.

[0135] Moreover, the gate dielectric film of the first transistor consists of thermal oxidation film which grew up to be the front face of a semi-conductor substrate. When the gate dielectric film of the second transistor becomes the front face on which at least one of the argon of a semi-conductor substrate, fluorine, and the fluorides was poured in from the gate dielectric film of the first transistor, and the thermal oxidation film which grew up to be coincidence The thermal oxidation film which grew up to be the front face of the semi-conductor substrate with which at least one of an argon, fluorine, and the fluorides was poured in Since it becomes a thick film from the thermal oxidation film which grew up to be coincidence on the front face which is not poured in The gate oxide of the second transistor can be formed in a thick film from the gate oxide of the first transistor, and the second transistor can be manufactured by the easy approach for a start the thickness of gate dielectric film is different from.

[0136] Moreover, the gate dielectric film of the second transistor consists of thermal oxidation film which grew up to be the front face of a semi-conductor substrate. When the gate dielectric film of the first transistor becomes the front face of the semi-conductor substrate with which at least one side of an indium and nitrogen was poured in from the gate dielectric film of the second transistor, and the thermal oxidation film which grew up to be coincidence The thermal oxidation film which grew up to be the front face of the semi-conductor substrate with which at least one side of an indium and nitrogen was poured in Since it becomes a thin film from the thermal oxidation film which grew up to be coincidence on the front face which is not poured in The gate oxide of the first transistor can be formed in a thin film from the gate oxide of the second transistor, and the second transistor can be manufactured by the easy approach for a start the thickness of gate dielectric film is different from.

[0137] By supplying only operation mode to the first processing circuit by the first electronic-circuitry device of this invention, although body power will be supplied to a power source from a dc-battery and the firm gas of the supply voltage will be carried out to the second processing circuit, if an electric power switch is turned on Although actuation is a low speed since gate dielectric film does not have ****** as for the second transistor A standby mode is also driven in the condition with a very small gate leakage current. The first transistor Since only operation mode is driven in the condition of operating at a high speed although a gate leakage current is not very small since gate dielectric film is the maximum ** and the second transistor is optimized for a start corresponding to an application or the engine performance, high-performance-izing and power-saving are compatible.

[0138] Although a low-battery power source supplies an electrical potential difference A (=B) to the second processing circuit for a start [of an integrated circuit device] and a high-voltage power source supplies an electrical potential difference C to the third processing circuit by the second electronic-circuitry device of this invention Since this second processing circuit controls the

existence of actuation of the first processing circuit corresponding to the notice of data of the notice means of data when the notice means of data gives the data notice of the predetermined data which can judge the necessity of actuation of the first processing circuit in the second processing circuit It is compatible in high-performance-izing and power-saving.
[0139] Although the thermal oxidation film is formed in the location of the second processing circuit for a start by the first circuit manufacture approach of this invention at coincidence By pouring in an argon, fluorine, and the fluoric acid-ized film, only the location of the second processing circuit Since the thermal oxidation film of the location of the third processing circuit which the thermal oxidation film of the location of the second processing circuit can make promote growth from the location of the first processing circuit, and consists of a bilayer is made into a thick film from the location of the second processing circuit "a<b<c" of the first transistor, the second transistor, and the third transistor -- the gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor substrate of a piece].
[0140] Although the thermal oxidation film is formed in the location of the second processing circuit for a start by the second circuit manufacture approach of this invention at coincidence By pouring in an indium and nitrogen, only the location of the first processing circuit Since the thermal oxidation film of the location of the third processing circuit which the thermal oxidation film of the location of the first processing circuit can make reduce growth from the location of the second processing circuit, and consists of a bilayer is made into a thick film from the location of the second processing circuit "a<b<c" of the first transistor, the second transistor, and the third transistor -- the gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor substrate of a piece].
[0141] since the location of the first processing circuit grows up the thermal oxidation film into proper thickness by the third circuit manufacture approach of this invention -- this -- a thermal oxidation mask -- covering -- the -- by growing up the thermal oxidation film into the location of the 2 third processing circuits Since the thermal oxidation film of the location of the third processing circuit which can form respectively the thermal oxidation film of the location of the second processing circuit in original thickness for a start, and consists of a bilayer is made into a thick film from the location of the second processing circuit "a<b<c" of the first transistor, the second transistor, and the third transistor -- the gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor substrate of a piece].

[0142] By the fourth circuit manufacture approach of this invention, since the location of the second processing circuit grows up the thermal oxidation film into proper thickness, by covering this with a thermal oxidation mask and growing up the thermal oxidation film into the location of the third processing circuit for a start Since the thermal oxidation film of the location of the third processing circuit where the thermal oxidation film of the location of the second processing circuit can form in original thickness respectively, and consists of a bilayer for a start is made into a thick film from the location of the second processing circuit "a<b<c" of the first transistor, the second transistor, and the third transistor -- the gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor substrate of a piece].
[0143] Moreover, in the above circuit manufacture approaches, the productivity of an integrated circuit device can be raised by forming the gate electrode of the first transistor from the conductive layer of the thermal oxidation mask formed in order to control the thickness of the gate dielectric film of the first transistor.
[0144] Moreover, since the polish recon film can prevent lower layer thermal oxidation good in physical properties and it can use as conductive layers, such as a gate electrode, by forming the conductive layer of a thermal oxidation mask by the polish recon film, the integrated circuit device of the good engine performance can be manufactured good.
[0145] By the fifth circuit manufacture approach of this invention, since the location of the first

processing circuit grows up the thermal oxidation film into proper thickness The thermal oxidation film is grown up into the location of the 2 third processing circuits. this -- the first polish recon film -- covering -- the -- From the conductive layer of the first polish recon film formed in order to control the thickness of the gate dielectric film of the first transistor, by forming the gate electrode of the first transistor Since the thermal oxidation film of the location of the third processing circuit which can form respectively the thermal oxidation film of the location of the second processing circuit in original thickness for a start, and consists of a bilayer is made into a thick film from the location of the second processing circuit "a<b<c" of the first transistor, the second transistor, and the third transistor -- the gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor substrate of a piece], and, moreover, the productivity of an integrated circuit device can also be raised.

[0146] By the sixth circuit manufacture approach of this invention, since the location of the second processing circuit grows up the thermal oxidation film into proper thickness Cover this by the first polish recon film, and the thermal oxidation film is grown up into the location of the third processing circuit for a start. From the conductive layer of the first polish recon film formed in order to control the thickness of the gate dielectric film of the second transistor, by forming the gate electrode of the second transistor Since the thermal oxidation film of the location of the third processing circuit which can form respectively the thermal oxidation film of the location of the second processing circuit in original thickness for a start, and consists of a bilayer is made into a thick film from the location of the second processing circuit "a<b<c" of the first transistor, the second transistor, and the third transistor -- the gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor substrate of a piece], and, moreover, the productivity of an integrated circuit device can also be raised.

[0147] By the seventh circuit manufacture approach of this invention, since the location of the first processing circuit grows up the thermal oxidation film into proper thickness The thermal oxidation film is grown up into the location of the 2 third processing circuits. this -- the first polish recon film -- covering -- the -- From the conductive layer of the first polish recon film formed in order to control the thickness of the gate dielectric film of the first transistor etching of the gate electrode which forms the gate electrode of the first transistor and is located in the front face of the gate oxide of the maximum ** of the first transistor -- the -- by performing separately from etching of the gate electrode of the 2 third transistor Since the thermal oxidation film of the location of the third processing circuit which can form respectively the thermal oxidation film of the location of the second processing circuit in original thickness for a start, and consists of a bilayer is made into a thick film from the location of the second processing circuit The gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor substrate of a piece]. "a<b<c" of the first transistor, the second transistor, and the third transistor -- And the productivity of an integrated circuit device can also be raised and the gate electrode of the third transistor can be further etched on the optimal conditions for each from the first.

[0148] By the eighth circuit manufacture approach of this invention, since the location of the second processing circuit grows up the thermal oxidation film into proper thickness Cover this by the first polish recon film, and the thermal oxidation film is grown up into the location of the third processing circuit for a start. From the conductive layer of the first polish recon film formed in order to control the thickness of the gate dielectric film of the second transistor By forming the gate electrode of the second transistor and performing separately from etching of the gate electrode of the third transistor for a start etching of the gate electrode located in the front face of the gate oxide of the maximum ** of the second transistor Since the thermal oxidation film of the location of the third processing circuit which can form respectively the thermal oxidation film of the location of the second processing circuit in original thickness for a start, and consists of a bilayer is made into a thick film from the location of the second processing circuit The gate dielectric film of thickness a-c which has satisfied relation can be formed easily [the front face of the semi-conductor

substrate of a piece]. "a<b<c" of the first transistor, the second transistor, and the third transistor -- And the productivity of an integrated circuit device can also be raised and the gate electrode of the third transistor can be further etched on the optimal conditions for each from the first.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the internal structure of the important section of the integrated circuit device of the first gestalt of operation of this invention.
[Drawing 2] It is the typical block diagram showing the whole integrated circuit device structure.
[Drawing 3] It is process drawing showing a part for the first portion of the circuit manufacture approach of the first gestalt of operation of this invention.
[Drawing 4] It is process drawing showing a part in the second half.
[Drawing 5] It is process drawing showing a part for the first portion of the circuit manufacture approach of the second gestalt of operation of this invention.
[Drawing 6] It is process drawing showing a part in the second half.
[Drawing 7] It is process drawing showing a part for the first portion of the circuit manufacture approach of the third gestalt of operation of this invention.
[Drawing 8] It is process drawing showing a part in the middle stage.
[Drawing 9] It is process drawing showing a part in the second half.
[Drawing 10] It is process drawing showing a part for the first portion of the circuit manufacture approach of the fourth gestalt of operation of this invention.
[Drawing 11] It is process drawing showing a part in the middle stage.
[Drawing 12] It is process drawing showing a part in the second half.
[Drawing 13] It is process drawing showing a part for the first portion of the circuit manufacture approach of the fifth gestalt of operation of this invention.
[Drawing 14] It is process drawing showing a part in the second half.
[Drawing 15] It is process drawing showing a part for the first portion of the circuit manufacture approach of the sixth gestalt of operation of this invention.
[Drawing 16] It is process drawing showing a part in the second half.
[Drawing 17] It is the property Fig. showing the relation between driver voltage and a gate leakage current.
[Description of Notations]
100 Integrated Circuit Device
101 Low-Battery Power Source
102 High-Voltage Power Source
111 First Processing Circuit

112 Second Processing Circuit
113 I/O Circuit Which is Third Processing Circuit
121 First Transistor
122 Second Transistor
123 Third Transistor
130 Gate Dielectric Film
131 Gate Electrode
141,144,163 Thermal oxidation film
142,143,151- 153, 162, and a 164,167,168,172 resist mask
161 First Polish Recon Film Which is Thermal Oxidation Mask and is Conductive Layer
166 Second Polish Recon Film

[Translation done.]

* NOTICES *

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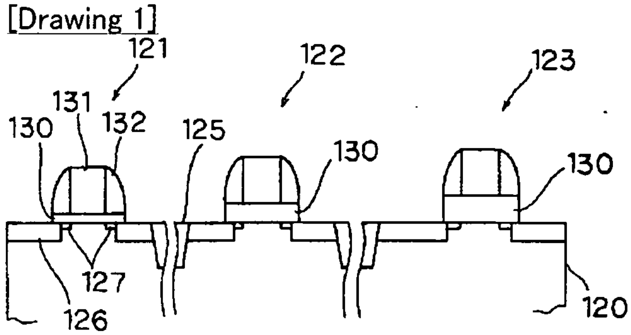
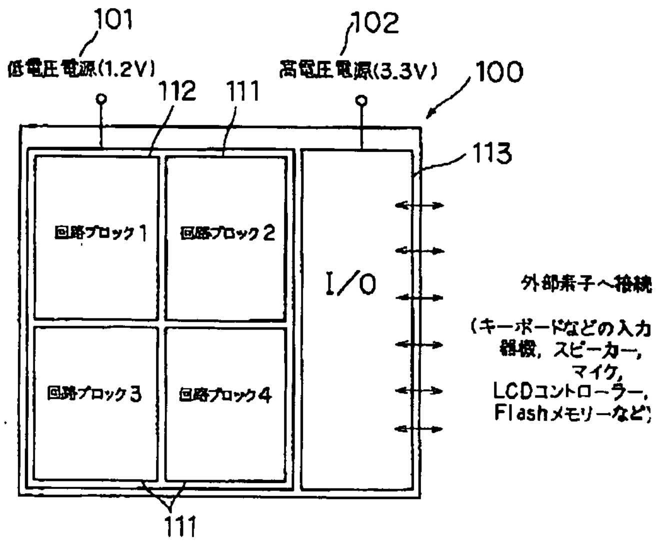
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

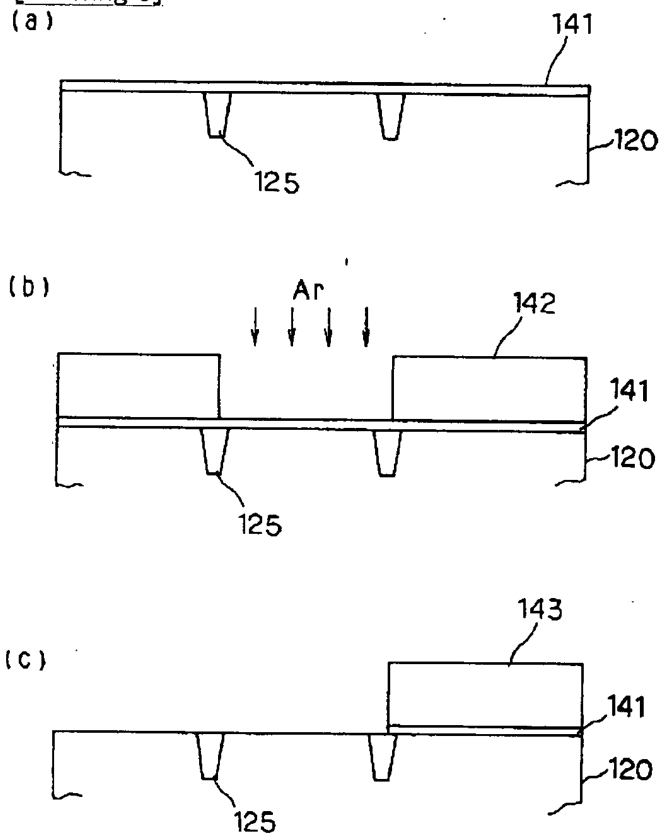
[Drawing 1]



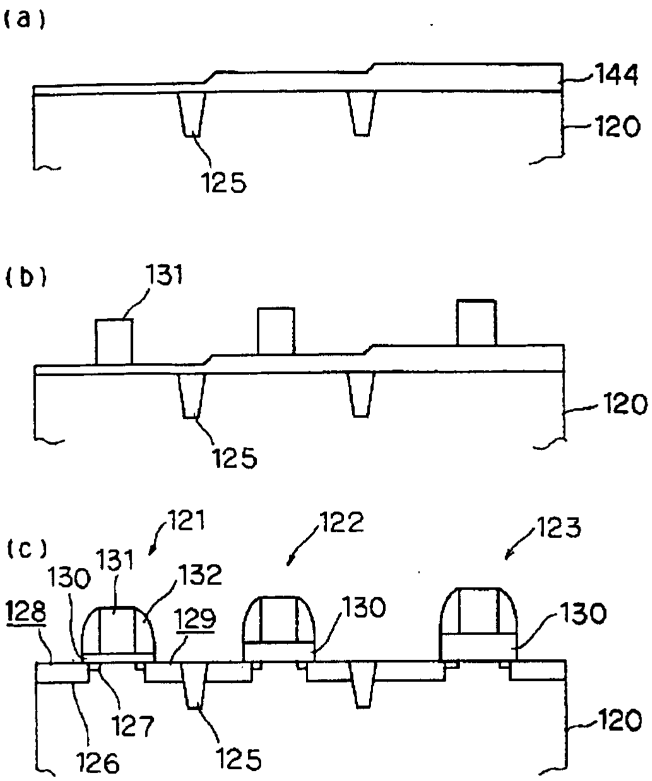
[Drawing 2]



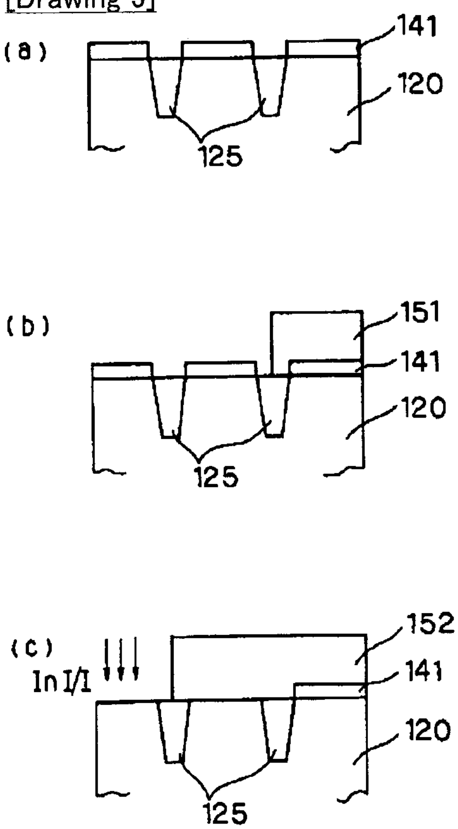
[Drawing 3]



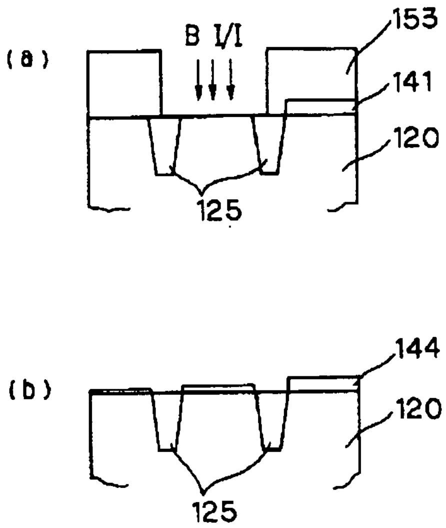
[Drawing 4]



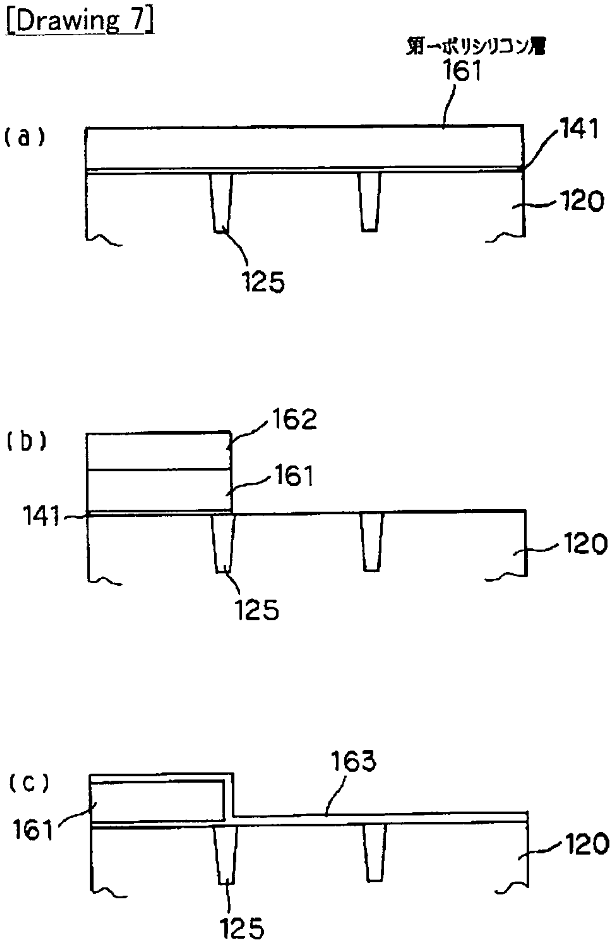
[Drawing 5]



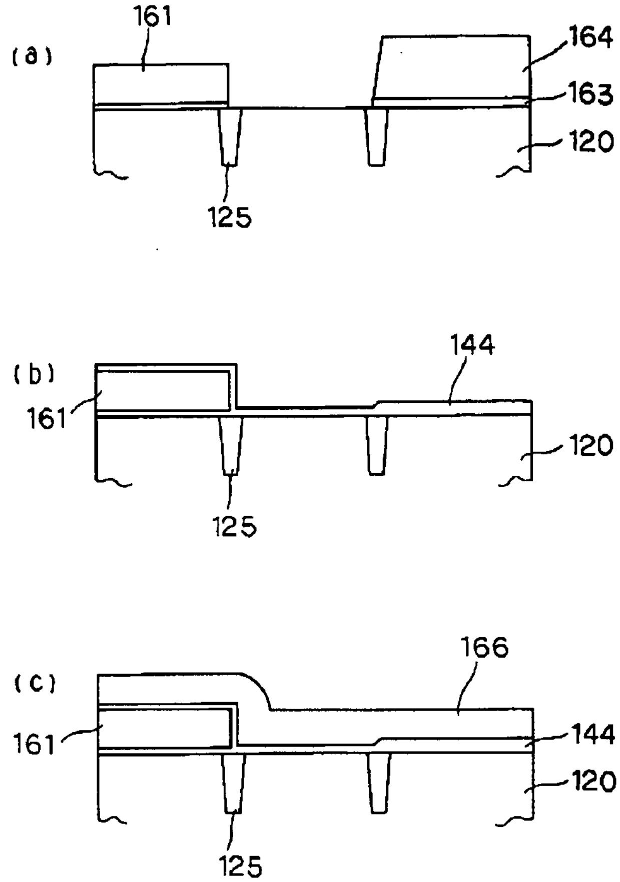
[Drawing 6]



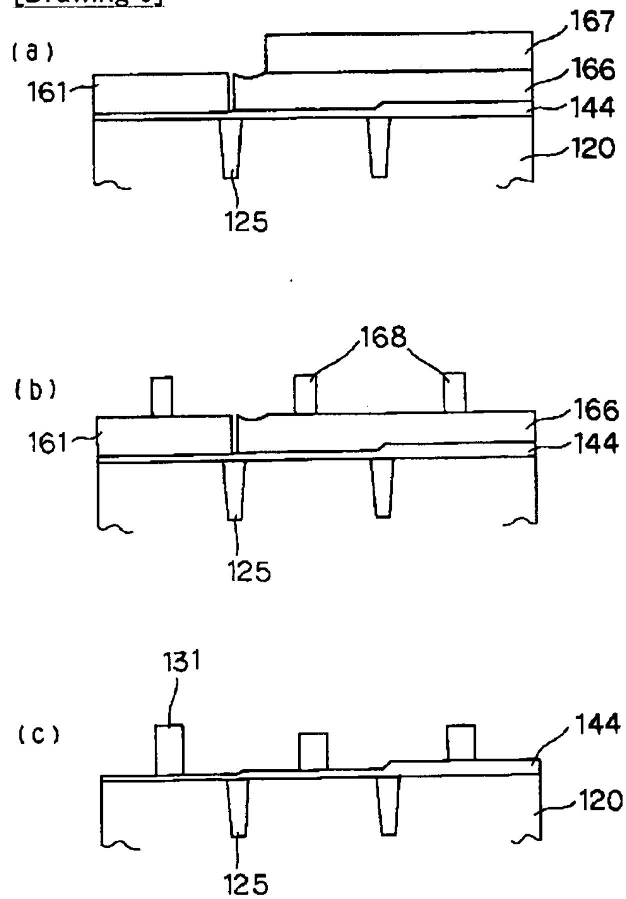
[Drawing 7]



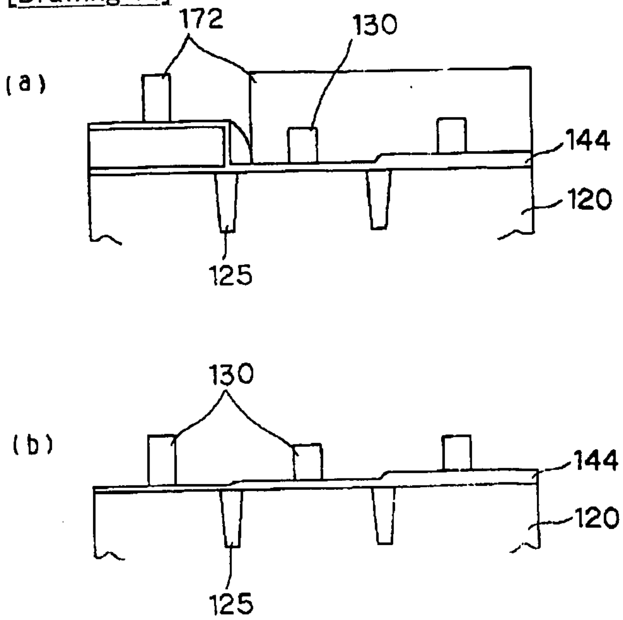
[Drawing 8]


(a)
161
164
163
120
125
(b)
144
161
120
125
(c)
166
161
144
120
125

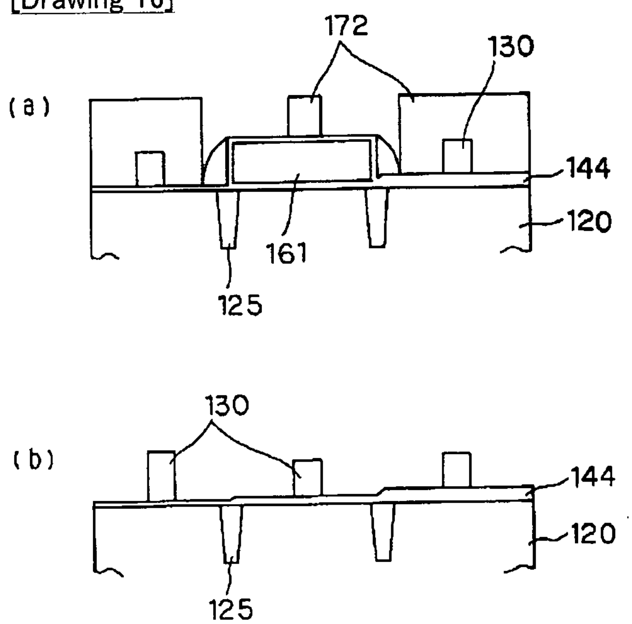
[Drawing 9]


(a)
167
161
166
144
120
125
(b)
168
166
161
144
125
(c)
131
144
120
125

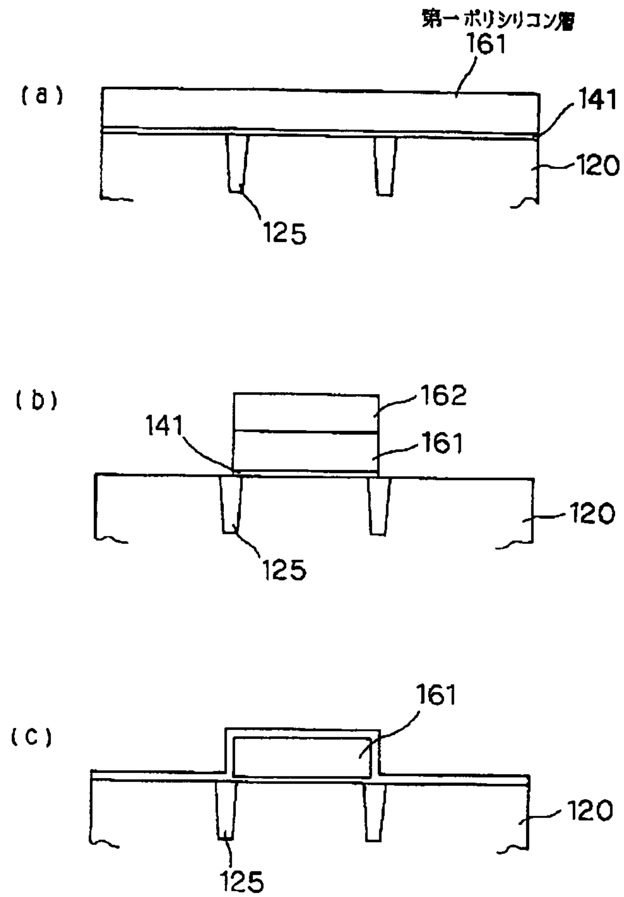
[Drawing 14]



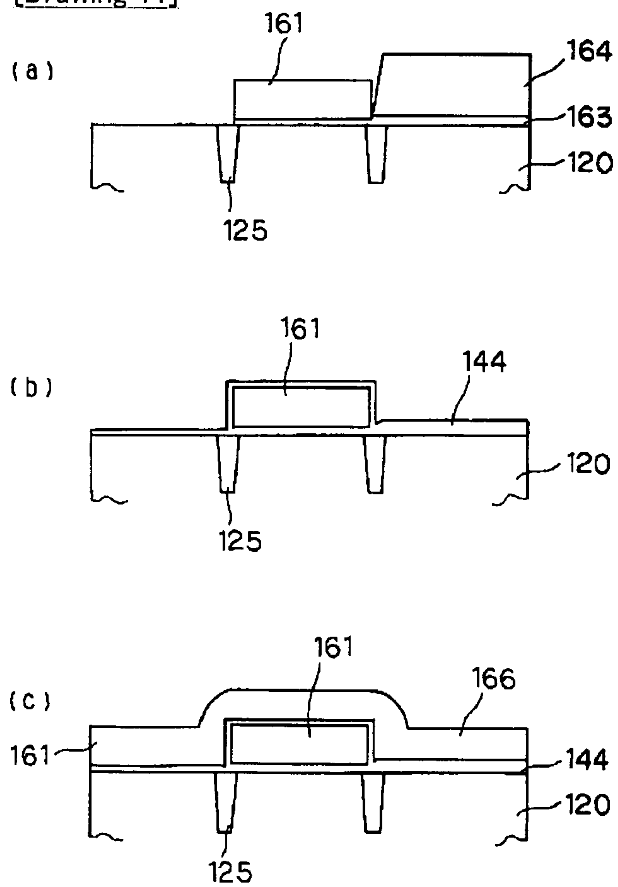
[Drawing 16]



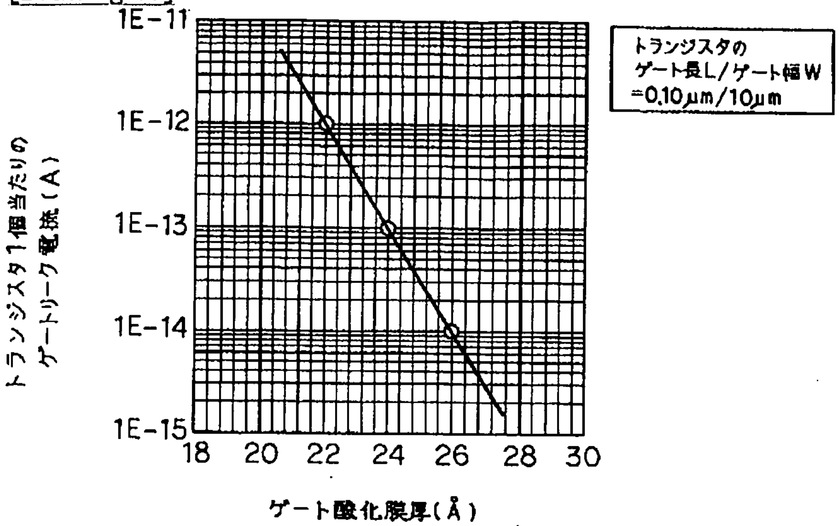
[Drawing 10]


第一ポリシリコン層
(a)
161
141
120
125
(b)
162
141
161
120
125
(c)
161
120
125

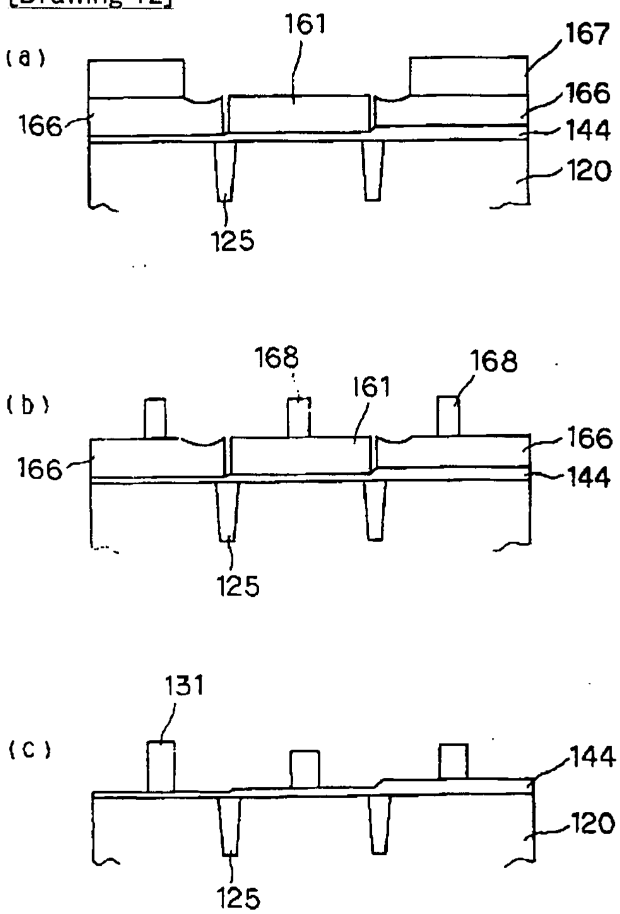
[Drawing 11]


(a)
161
164
163
120
125
(b)
161
144
120
125
(c)
161
166
161
144
120
125

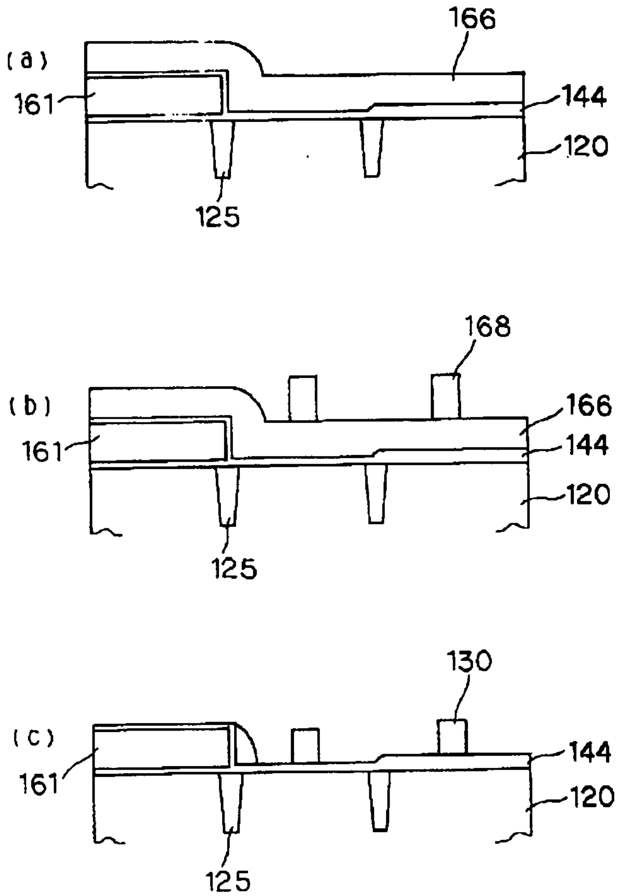
[Drawing 17]



[Drawing 12]

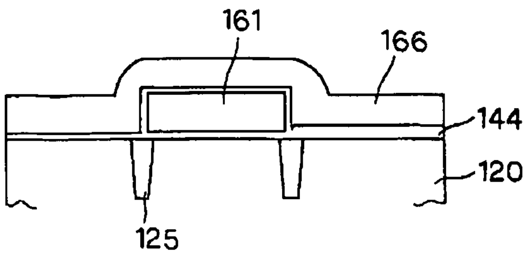


[Drawing 13]

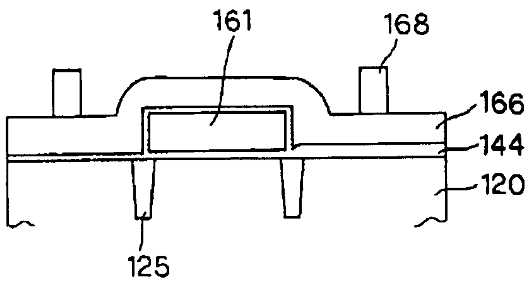

(a)
166
161
144
120
125
(b)
168
166
161
144
120
125
(c)
130
161
144
120
125

[Drawing 15]

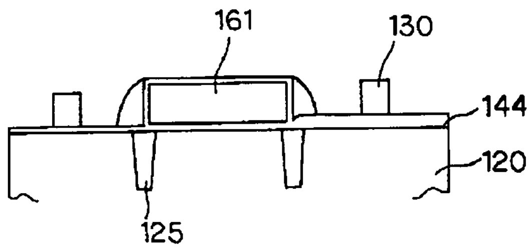
(a)



(b)



(c)



[Translation done.]